Low-Voltage Artificial Neuron using Feedback Engineered Insulator-to-Metal-Transition Devices

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Abstract

We demonstrate a solid-state spiking artificial neuron based upon an insulator-to-metal (IMT) transition material element that operates at an unprecedented low voltage (0.8 V). We have developed a general coupled electrical-thermal device model for IMT based devices to accurately predict experimental outcomes. From the experiment and simulation, we show that voltage scalability to sub 0.3 V is possible by scaling of the IMT based neuron.

Background

Insulator-to-metal-transition (IMT) materials exhibit the property of an abrupt, reversible resistivity change as a function of temperature [1,2] and have recently attracted significant research attention as device elements [3,4], applicable for neuromorphic circuits and architectures. There is however a lack of a systematic approach for designing such devices and circuits and the absence of a clear device model for IMT materials.

Two key device elements in a neuromorphic circuit are the neuron and the synapse. A CMOS implementation of a neuron typically requires 8 or more active components in order to demonstrate two of the key aspects of a neuron: (i) an "integrate-and-fire" capability that integrates input signals followed by the release of a threshold activated output waveform, and (ii) a post output refractory period during which the neuron does not integrate inputs. Earlier work on non-silicon neurons have employed phase change materials (PCM), and vanadium oxide (VO_2) layers coupled with MOSFETs [5,6]. These devices typically required high voltages for operation (e.g.>5 V for resetting PCM) [6]. There has also been work on a "neuristor" using memristor elements that turn on at ~1.7 V and which use more complex circuitry requiring two voltage inputs and several elements [7].

Using VO_2 as a prototypical IMT material we experimentally demonstrate an artificial neuron with integrate-and-fire and post firing refractory period characteristics which can operate at an unprecedented low voltage (0.8 V). It employs a a novel design that uses just two elements, does not require a transistor, and utilizes the dynamic interplay between electrical charging and thermal engineering to offer a wide design space in its input/output characteristics. Finally, we have developed a first-order device model for using IMT elements which captures the coupled electrical-thermal feedback for predicting device performance and exploration of the design space. The model indicates that our approach is scalable in voltage and sub 0.3 V operation is possible.

Device Fabrication

VO_2 thin films (~200 nm) were deposited on both SiO_2/silicon and c-axis sapphire substrates by vacuum sputtering at deposition temperatures between 775K – 875K. It is well known that the strength of the IMT transition (defined as the ratio of the resistivities at room temperature and at 400 K and denoted by ρ_{rH}/ρ_{rL}) in VO_2 can be controlled by varying deposition conditions and is related to the oxygen stoichiometry [1]. In this manner VO_2 films with a wide range IMT strengths, with ρ_{rH}/ρ_{rL} varying over five orders of magnitude were fabricated (**Fig. 1**). One should note that the high resistance states have different values for the different films–this plays a critical role in achieving low voltage operation. A representative cross-sectional transmission electron microscope image of a typical VO_2 layer grown on Si/SiO_2 is shown in **Fig. 2**. Lateral VO_2 strips were subsequently fabricated by Cl_2-based reactive ion etching. Evaporated Ti/Au pads at either end of the VO_2 strip was used for electrical contacts (**Fig. 3** inset). The length and width of the VO_2 strip was varied from 0.5 to 20 μm. Transmission line measurements (TLM) were conducted (**Fig. 3**) for samples B and C (see **Fig. 1**) to show that the contact resistance is negligible for the devices and to also verify that the sheet resistances were consistent with the resistivity-temperature measurements of **Fig. 1**.

IMT Device Model

Although the detail transition switching mechanisms of IMT can be rather complicated [8], a simplified model based on positive feedback can be developed and used for compact circuit design. The temperature triggered resistivity switching under joule heating in an IMT material such as VO_2 operates via a positive feedback mechanism: once the dissipated electrical power (=V^2/R, where V is the applied voltage and R is the resistance) raises the IMT element temperature beyond the IMT threshold, the subsequent drop in resistance further increases the dissipated power and Joule heating of the element. Its design characteristics are determined by the coupled electrical and thermal physics for an IMT material as formulated below for the strip geometry of the device (with a rectangular cross-section) shown in **Fig.4**. It includes the physics of joule heating, negative differential resistance (NDR), heat transfer and the positive feedback that arises from their interplay. We use a one dimensional model and assume that the temperature in the bar varies only along its length. The IMT model can be integrated with passive element and transistor models for hybrid circuit simulation.

$$\mu\rho_d A\frac{\partial T}{\partial t} = KA\frac{\partial^2 T}{\partial x^2} + I^2\rho_r(x,T) - h\cdot[T - T_a] \qquad \text{(Eq. 1)}$$

$$I = \frac{V}{R_{IMT} - R_S} \qquad \text{(Eq. 2)}$$

$$R_{IMT} = \int_{-L/2}^{L/2}\frac{\rho_r(x,T)}{A}dx \qquad \text{(Eq. 3)}$$

The physical parameters used in the equations are described in **Table I**, along with specific values used for the device simulations (relevant to VO_2). All simulations will follow these parameters unless specified otherwise. The resistivity ρ_r is modeled by a look-up table based on the data in **Fig. 1**. The last term in **Eq. 1** captures the convective heat transfer between the IMT surface and the ambient. Radiative

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heat transfer is ignored since it is negligible at the temperatures under consideration. **Fig. 5** shows the transient temperature profile in the IMT device as a function of time as two representative voltages are applied across it which are below and above (**Fig. 5**) the critical voltage (V_c) required to trigger the IMT transition from a resistivity of ρ_{rH} to ρ_{rL}. The temperature and resistance switching of IMT from the simulation is shown in **Fig. 6**. Our model indicates that there are two critical voltages for the forward (ρ_{rH}-to-ρ_{rL}) and backward (ρ_{rL}-to-ρ_{rH}) switching. They are denoted as V_{cF} and V_{cB} and they play a key role in the voltage required for device operation (**Fig. 7**).

Our simulations identify three key device design parameters (**Fig. 8**). Firstly, the high resistive state ρ_{rH} plays a significant role in the value of the critical voltage and hysteresis. V_{cB} and V_{cF} are dependent upon ρ_{rL} and ρ_{rH} respectively. By reducing ρ_{rH}/ρ_{rL}, $V_{c,H}$ can be dramatically reduced. For instance, V_{cF} is 0.9 V for ρ_{rH}/ρ_{rL} ~10^1, but increases beyond 10 V when ρ_{rH}/ρ_{rL}~ 10^4. Secondly, the convective heat transfer dominates the heat loss through the sidewall. When the heat transfer coefficient h is close to zero, V_{cF} reduces to 0.6 V for the device geometry used. Hence, heat insulation is important for low voltage application. In this work, a photoresist coating is used on the IMT device as an insulating sheath. Thirdly, the device length significantly affects $V_{cF,}$ roughly following an expected linear V_{cF} vs. L relationship. On the other hand, the backward critical voltage V_{cB} depends upon the additional series resistance, because at a low resistance state, the current must be limited to avoid destroying the device. In summary, the lowest V_{cF} and therefore the lowest operating voltage can be achieved by reducing ρ_{rL}, h and L.

The model is tested against experiment and shows excellent consistency. **Fig.9** shows the transient measurement of the fabricated IMT device (L=2 μm, W=2.5 μm) with a DC bias slightly above V_{cF} at t=0. The switching occurs after ~ 0.5 μs. This agrees well with the time scale predicted by the model (**Fig. 6**). Additionally, **Fig. 10** shows the measured V_{cF} vs. L for sample C. All parameter values chosen, except L, follow the baseline values in **Table I**. The experimental values of V_{cF} from **Fig. 10** validates the simulated value of V_{cF} as a function of L. Comparing the experimental data in **Fig. 11** and **Fig. 1** for samples A,B and C, we find that the higher the IMT strength, the larger the hysteresis. This is consistent with our simulation results (**Fig. 8a**) where the difference between V_{cF} and V_{cB} is the hysteresis.

Artificial Spiking Neuron

We construct the artificial neuron circuit as shown in **Fig. 12**. In simulation, the IMT strip is connected in parallel with a capacitor (C_o=1 nF). The input signal is a current source that is applied to the left node (I_{in}). As shown in **Fig. 13a**, two input current pulse trains are fed to the left node. Each one consists of 10 pulses (pulse width 100 ns) with a magnitude of 2 mA. Because the RC time constant at the high resistive state, τ_H, is much longer than the total integration timeframe, the current leakage through the IMT is small compared to the capacitance charging rate when the device is in its insulating state. As the charge across the capacitor increases, the voltage at the left node increases (**Fig. 13b**). When the voltage rises beyond V_{cF} (at the 6th pulse in **Fig. 13a**), transition is triggered (**Fig. 13c**). This results in a sharp output current (**Fig. 13d**) and the voltage at the left node quickly drops close to ground voltage. After it fires, due to the excess joule heating, the IMT remains at its lower resistive state for a time period of t_T during which time any input current pulses are directly drained by the IMT resistance. The charge integration in the capacitor during this time is virtually zero. *This characteristic mimics the post-firing refractory period in a biological neuron*. The charge integration in C_o is possible only when the refractory period is over and the IMT returns to its high resistivity state as it cools down below the transition temperature. Controlling the heat transfer characteristics then allows a way to control the post-firing refractory period time.

In our experiment, we constructed two artificial neuron circuits using the devices shown in **Fig. 11** for samples B and C. The measured characteristics of the neurons are shown in **Fig. 14**. They each received input current pulses starting from t=0. Both circuits exhibit the first firing at comparable times (t= 0.35 ms for sample B and and t=0.3 ms for samples C) but at very different voltages: sample B fired when the voltage across the capacitor was ~2 V, compared to ~0.8 V for sample C. This tracks the measured value of V_{cF} in the respective devices (**Fig. 11**) when the device switches to the low resistive state. The current output (**Figs. 14b, d**) represents the temporal firing action of the neuron. During this time, the capacitor is discharged through the low resistive state. The firing pattern is enlarged in the inset of **Fig. 14a**. There is a short period (t_R~10 μs) during the tail end of the firing that the IMT remains in a low resistive state. This is the refractory period as explained earlier. The time scale of the neuron firing frequency can be tuned by altering the capacitor values. For the results shown here, both circuits use 10 nF capacitors. With large capacitances we have achieved slower neurons with millisecond firing periods.

Voltage scaling is a key aspect for feedback engineering of IMT device as low voltage operation is desirable for energy efficiency electronics. Since our model closely match the experimental result, we can use it to predict the scalability of the IMT devices. **Fig. 15** shows that one can reduce the heat loss (h) and the length (L) of the IMT for sub 0.3 V operation. Currently, our experimental IMT device with 2.5 μm width and 0.5 μm length has the maximum operating voltage of 0.8 V. This is so far the lowest among the maximum voltage appeared in spiking neuron circuits (**Table II**).

Conclusions

We have developed a general electrical-thermal model for IMT based devices, verified it against electrical measurements of VO_2 devices, and then used it for designing IMT based artificial neurons. Based upon this we have experimentally demonstrated an artificial neuron with integrate-and-fire and post firing refractory period characteristics and which can operate at an unprecedented low voltage of 0.8 V. Finally, we show via our simulations that further voltage reduction is possible through IMT device scaling to sub 0.3V.

Acknowledgements

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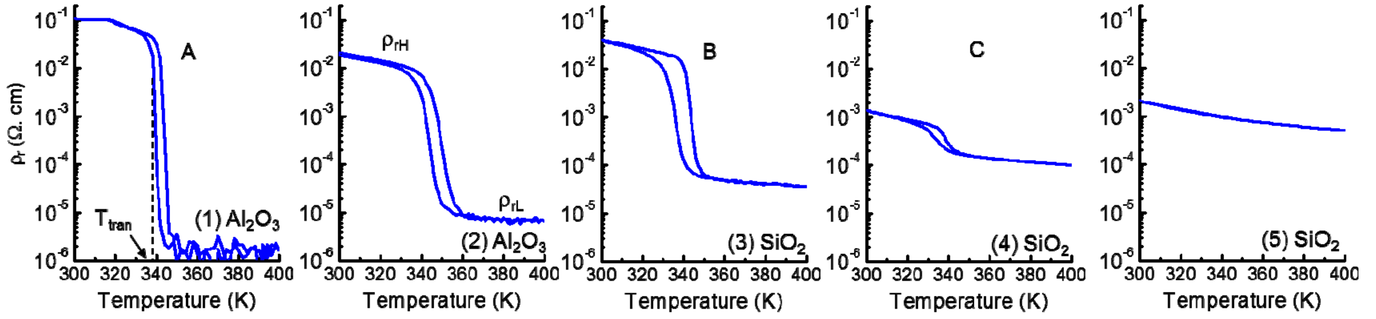

Fig. 1 Measured resistivity vs. temperature of VO_2 grown on different substrate and different conditions. VO_2 on Al_2O_3 exhibits the largest IMT strength. The IMT strength are (1) 8×10^4, (2) 2×10^3, (3) 1×10^3, (4) 2×10^1, and (5) 3. Sample A, B and C are used for IMTs device fabrications. Transition temperature (T_{tran}), high and low resistivity state (ρ_{rH}, ρ_{rL}) are labeled in the figures.

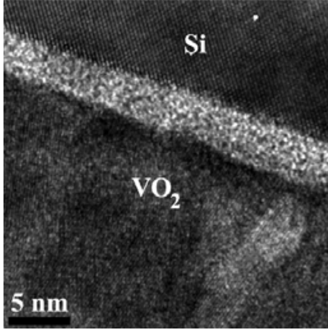

Fig. 2 TEM image of VO_2 grown on Silicon under similar condition as this work.

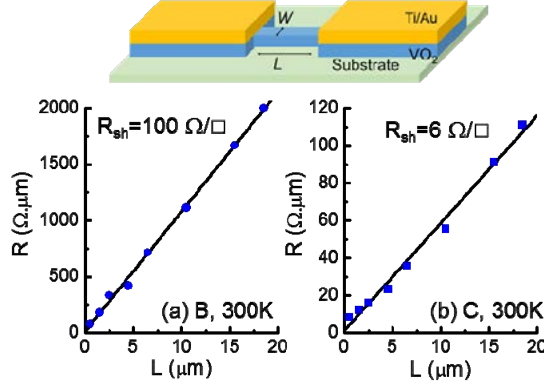

Fig. 3 TLM measurement at room temperature for two types of VO_2 films on sample A and B. Inset shows the contact scheme.

Table I: Baseline model parameters

Parameter	Symbol	Value
Thermal conductivity	K (W/K-m)	6
Specific heat capacity	C* (J/K-kg)	690
Effective convective heat transfer coefficient	h (W/K-m^2)	10
High resistivity state	ρ_{rH} (Ω-m)	10^{-3}
Low resistivity state	ρ_{rL} (Ω-m)	10^{-5}
Density	ρ_d (kg/m^3)	4×10^3
Area	A (m^2)	5×10^{-13}
Width	W (m)	2.5×10^{-6}
Length	L (m)	2×10^{-6}
Ambient temperature	T_a(K)	300
Series resistance	Rs (Ω)	200

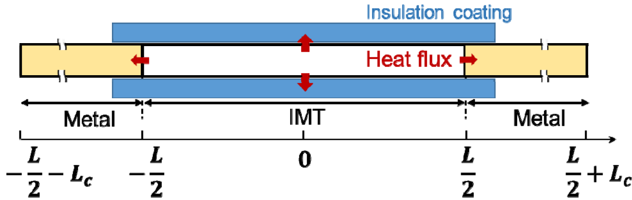

Fig. 4 Schematic illustration for the simulation. The IMT of length L is connected to two external long metal contacts that serve as heat sinks. IMT is coated with resist for heat insulation; therefore heat loss through sidewall can be minimized.

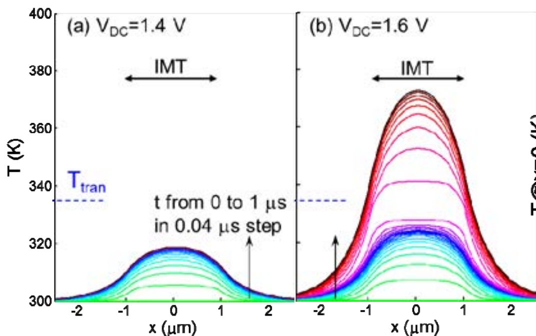

Fig. 5 Simulated temperature profile in IMT device and portion of the contacts in the first 1 μs after DC voltage (V_{DC}) is applied at two ends. (a) For V_{DC}=1.4 V, IMT does not switch. (b) For V_{DC}=1.6 V IMT switches. T_{tran} is defined in Fig. 1. Baseline parameters are used (Table I).

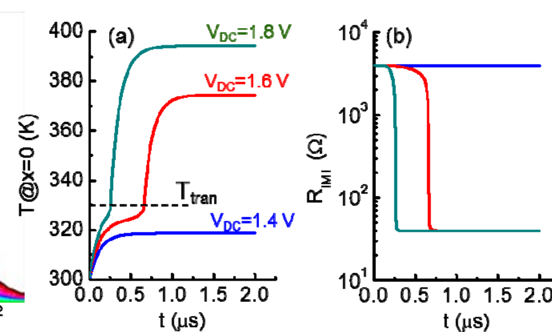

Fig. 6 (a) Simulated temperature at the center of the IMT device and (b) R_{IMT} after V_{DC} is applied. IMT switching occurs at a time scale of t=0.1 to 1 μs based on the electrical-thermal model. Baseline parameters are used (Table I).

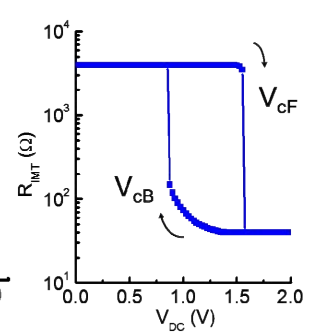

Fig. 7 Simulated R_{IMT} (resistance extracted from the two ends of the bar) vs. V_{DC}. The critical voltages are labeled.

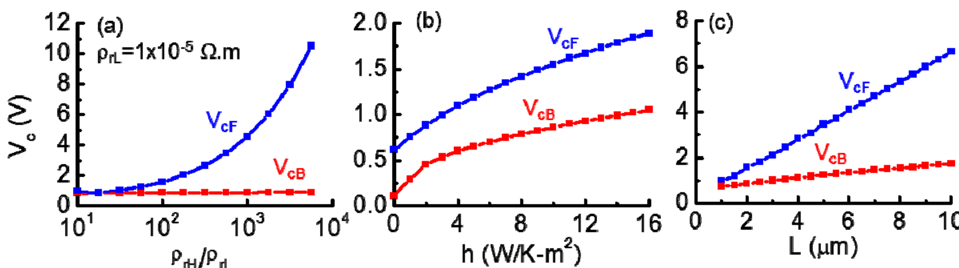

Fig. 8 Simulated critical voltages for three key design parameters: (a) IMT strength: ρ_{rL} is fixed at 1×10^{-5} Ω.m and the ratio of ρ_{rH}/ρ_{rL} varies, (b) effective convention heat transfer coefficient, h, (c) device length. Only the parameter in the x-axis is treated as variable. Other device parameters are listed in Table I.

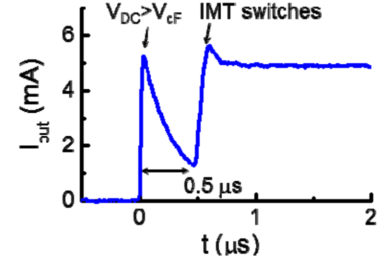

Fig. 9 Measured transient current of IMT switching after a step voltage is applied at t=0. Switching occurs at t=0.5 μs. The step voltage is slightly higher than IMT's V_{cF}. Device length and width are 2 μm and 2.5 μm respectively.

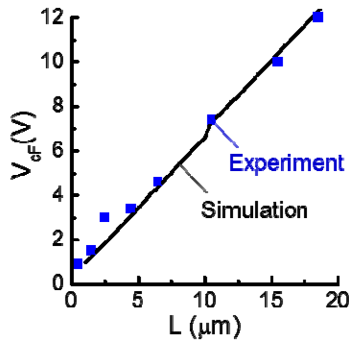

Fig. 10 Measured (blue) and simulated (black) V_{cF} vs. IMT device length for sample C. The experiment and simulation shows excellent agreement. Device width is 2 μm.

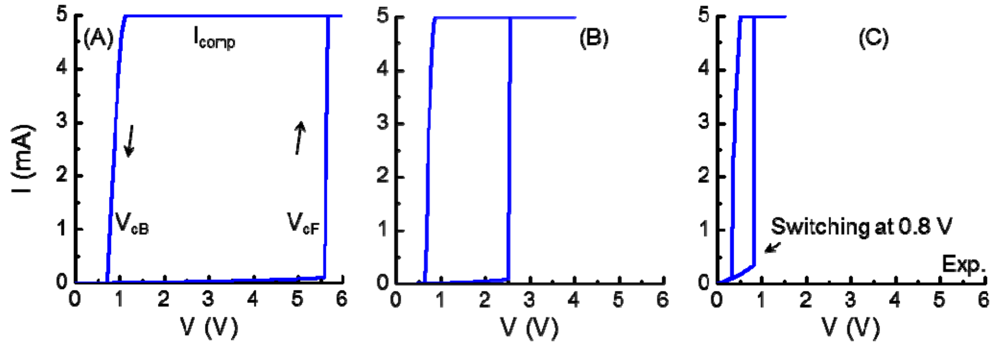

Fig.11 Measured hysteresis loop for VO_2 on sample A, B and C. Large V_{cF}-V_{cB} is observed in A due to its high ρ_{rH}/ρ_{rL} Sub 0.8 V switching is obtained in C. The current compliance (I_{comp}) is set at 5 mA. Device length and width are 0.5 μm and 2.5 μm respectively.

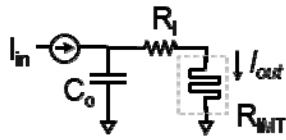

Fig. 12 Circuit schematics of combining IMT (dashed box) with capacitance and current source for demonstrating artificial firing neurons. A resistor is connected in series to limit the current through the IMT and measure current output.

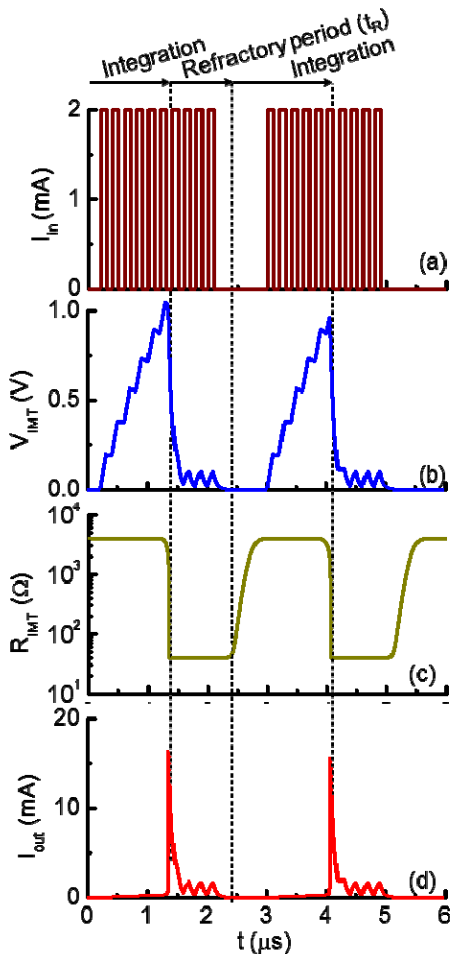

Fig. 13 Simulated waveforms for circuit in Fig. 12: (a) Input current pulse trains, (b) Voltage across the IMT device. (c) Resistance of the IMT device. (d) Current through IMT device. Device length is L=0.5 μm. Other parameters follow the baseline (Table I).

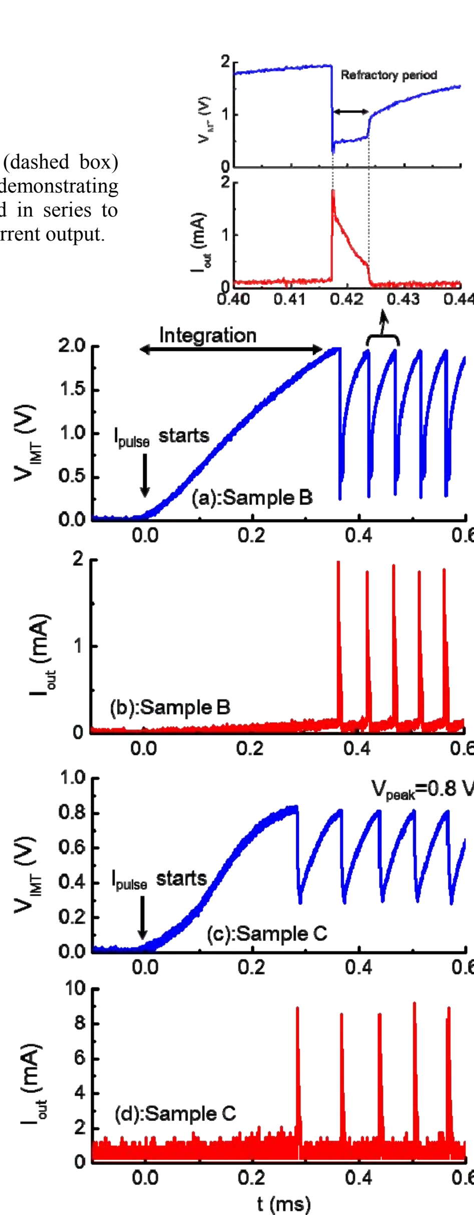

Fig. 14 Measured waveforms for circuit in Fig. 12. (a) voltage across the IMT and (b) the current through the IMT for sample B. (c) voltage across the IMT and (d) the current through the IMT for sample C. Inset shows the enlarged view for sample B.

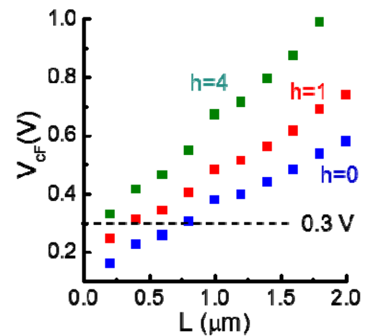

Fig. 15 Simulated Forward Critical Voltages for IMT device with L and h as variable. Other parameters follow the baseline. When L shrinks below 0.4 μm and low heat loss through the sidewall, sub 0.3 V switching is feasible.

Table II: Comparison with recent literatures on non-silicon spiking neurons

	This work	[5]	[6]	[7]
Material	VO_2	VO_2	PCM	Mott Insulator
Maximum voltage in operation†	0.8 V	1 V	5.3 V*	1.7 V**
Need active devices?	No	Yes	No	Yes

† This is the maximum voltage in operation reported in respective neuron circuits.
* Reset pulse voltage for PCM.
** The knee turn-on voltage from I-V measurement on isolated device.

References

[1] D. Ruzmetov, et. al, Physical Rev. B, 77, p. 195442, 2008.
[2] J. Yoon, et. al, ACS Appl. Mater. Interfaces, vol. 8, no. 3, pp. 2280–2286, 2016.
[3] H. Madan, et. al, IEDM 2015, pp. 9.3.1–9.3.4.
[4] N. Shukla, et. al, Nature Commun., vol. 6, p. 7812, 2015.
[5] M. Jerry, et. al, Device Research Conference 2016.
[6] T. Tuma, et. al., Nature Nanotechnology, 11, pp. 693–699, 2016.
[7] M. D. Pickett, et. al, Nature Materials, pp. 114-117, 2012.
[8] S. D. Ha, et. al, J. Applied Physics vol. 113, p. 184501, 2013.