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Silicon compatible Sn-based resistive switching memory†

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Large banks of cheap, fast, non-volatile, energy efficient, scalable solid-state memories are an increasingly essential component for today's data intensive computing. Conductive-bridge random access memory (CBRAM) – which involves voltage driven formation and dissolution of Cu or Ag filaments in a Cu (or Ag) anode/dielectric (HfO_2 or Al_2O_3)/inert cathode device – possesses the necessary attributes to fit the requirements. Cu and Ag are, however, fast diffusers and known contaminants in silicon microelectronics. Herein, employing a criterion for electrode metal selection applicable to cationic filamentary devices and using first principles calculations for estimating diffusion barriers in HfO_2, we identify tin (Sn) as a rational, silicon CMOS compatible replacement for Cu and Ag anodes in CBRAM devices. We then experimentally fabricate Sn based CBRAM devices and demonstrate very fast, steep-slope memory switching as well as threshold switching, comparable to Cu or Ag based devices. Furthermore, time evolution of the cationic filament formation along with the switching mechanism is discussed based on time domain measurements (*I vs. t*) carried out under constant voltage stress. The time to threshold is shown to be a function of both the voltage stress (V_{stress}) as well as the initial leakage current (I_0) through the device.

Resistive switching devices[1,2] that rely on formation of an electric field driven conductive metallic filament in a dielectric layer are being extensively studied for non-volatile memory,[3] as non-volatile switches in reconfigurable circuits[4] and as synaptic elements in biologically inspired computing applications.[5,6] These device structures typically employ a dielectric oxide thin film such as HfO_2 or Al_2O_3 [3,7] (as switching matrix) and an inert (W or Pt) cathode and an electrochemically active (Cu or Ag) anode on either side of it. Under voltage bias, electrochemical migration of Cu or Ag ions from the anode leads to a propagating conducting filament between the cathode and anode, leading to a non-volatile change in the resistance of the device. These devices, often referred to as conductive-bridge random access memory (CBRAM) devices, offer large (up to 10 orders of magnitude) high/low resistance ratio[8] and excellent (low) cycle-to-cycle (C2C) variability.[7]

Typical CBRAM type devices studied to date have been based on the diffusion of Cu and Ag ions for filament formation. However, these metals are known fast diffusers in silicon (see Fig. 1(a)) and references[9–11] and present the risk of severe contamination when integrated into silicon circuitry. Overcoming this issue requires introduction of diffusion barriers (as is done in Cu interconnect technology[12]), in turn limiting design options and increasing complexity. For instance, in the cases where the memory element is connected in series with a silicon transistor or a selector device in order to suppress leakage currents, a fast diffuser such as Cu or Ag risks contaminating the transistor or selector.

In this study, we present a criterion – based on established and computed materials parameters – for electrode metal selection applicable to cationic filamentary devices. Using this criterion, we argue that a metal – such as Sn – can be used instead of Cu or Ag as the cationic filament forming element in CBRAM structures. We then report successful fabrication and reversible resistance switching using Sn as the anode in CBRAM devices, thereby ratifying our predictions. Unlike the aliovalent Cu and Ag, which create electronically active defect centers in Si, Sn offers the major advantage in being CMOS friendly: it is isovalent with Si and can be incorporated in significant amounts on Si substitutional lattice sites without creating electrically active defects.[13] It is also a slower diffuser in Si than Cu and Ag, for comparable temperature ranges, reducing contamination risk (see Fig. 1(a)).

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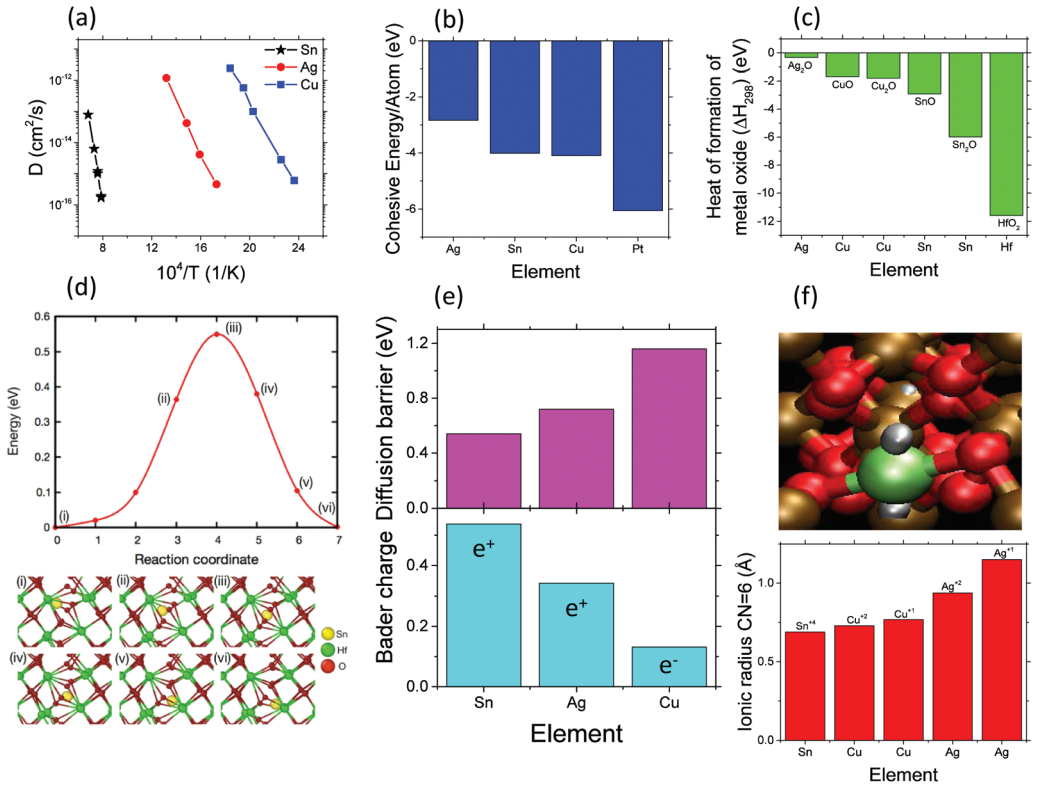

Fig. 1 Comparison of (a) diffusion coefficient for Sn,[11] Ag[10] and Cu[9] in Si. (b) Cohesive energy[14] for Ag, Sn, Cu and Pt, (c) heat of formation of metal oxide[15] for Ag, Sn, Cu and Hf. (d) Diffusion energy barriers for Sn in monoclinic HfO_2 computed using Nudged-elastic band (NEB) density functional theory (DFT) calculations along the most preferred diffusion pathway. (Bottom) Selected configurations from the pathway are labeled (i)–(vi). The most preferred pathway for Sn diffusion in pristine HfO_2 is *via* hopping from one octahedral interstitial site to its nearest octahedral interstitial site (O–O). Sn occupies interstitial sites in HfO_2 in the initial and final configurations (i and vi). The migration of Sn involves distortion of Hf–O–Hf bonds resulting in the barrier state depicted in (iii). (e) (Top) DFT derived diffusion barriers and (Bottom) Bader charges for Sn, Ag and Cu in HfO_2. (f) (Top) Charge density difference plots between HfO_2 and Sn of the transition state for the Sn diffusion in HfO_2. The lime, red and ochre spheres represent Sn, O and Hf respectively. The silver surface indicates the depleted charge. The isosurface plotted is 0.12e $Å^{-3}$. (Bottom) Ionic radius[16] for Sn, Cu and Ag.

So far, in the case of cationic filamentary devices, resistive switching phenomenon has been demonstrated in many oxides, chalcogenides (sulfides, iodides, selenides, tellurides, ternary chalcogenides) and others (methylsilsesquioxane (MSQ), doped organic semiconductors, nitrides, amorphous Si, Carbon, vacuum gaps). An exhaustive list can be found in the review article[17] and references therein. However, all the above listed demonstrations have involved changing the insulating matrix while restricting the anode (filament forming) metal to Cu or Ag. We developed a criterion – consisting of three material parameters – that not only justifies the use of Cu or Ag as most common anode for cationic filamentary devices but also allows exploration of other viable candidate metals for such applications. Finding newer anode metal would allow more combinations in finding out better performing devices and devices with suitable peculiar characteristic features and functionality. We explain the criterion next.

For low energy switching of non-volatile memory that relies upon filament formation, we have to consider three components related to the energetic cost of creating a filament across the Metal–Insulator–Metal (MIM) stack. If the anode is in direct contact with the dielectric oxide, there is the energy cost of moving the metal atoms from the anode into the dielectric oxide. A simple indicator of this energy cost is the cohesive energy for the metal (E_c). If there is an interfacial anodic oxide layer between the anode metal and the dielectric, then one needs to consider the energy cost of extracting the metal atom from the anodic oxide: this is related to the heat of formation of anode metal oxide (ΔH). The third component is work done to transport the anode metal atom across the dielectric oxide to the cathode by drift driven diffusion. Assuming all other parameters for drift to be the same, in general, a smaller ionic radius will lead to a lower activation barrier for diffusion and is preferable. Thus, in general, for low energy cationic filament formation, smaller E_c of the anode metal, lower ΔH of anode metal oxide and smaller ionic radius are preferable. So far, Ag and Cu have been very common choice of anode metal for cationic filamentary devices due to their small E_c and low ΔH (Fig. 1(b and c)). However, this criterion can also be applied to other metals to determine their suitability for use as anode for low energy cationic filament formation. Based on this criterion we identified Sn as a viable candidate metal as follows. Fig. 1 (b and c) compare density functional theory (DFT) derived cohesive energies[14] and heat of formation of oxide[15] for Cu, Ag

and Sn. Cohesive energy of Sn is slightly higher than Ag but comparable to Cu. The heat of formation of SnO_2 is moderately higher than Cu_2O and Ag_2O. We then carried out DFT based first principles calculations in order to estimate the activation barrier for Sn diffusion within HfO_2. The results of the calculations (Fig. 1(d)) indicate that the activation barrier for Sn diffusion (~0.54 eV) within HfO_2 is lower than that for Ag (0.72 eV) and Cu (1.16 eV). To understand this low barrier for Sn, we compute the charge density difference and Bader charges for Sn at the transition state namely the highest total energy state as it diffuses from one interstitial site to another as shown in Fig. 1(e). Details regarding the most preferred atomistic diffusion pathway of Sn in HfO_2 are given in the ESI.† Compared to Cu and Ag, our calculations suggest a substantial amount of charge depletion for Sn at the transition state as it is repelled by its two nearest neighboring O atoms from both sides (see Fig. 1 (f-top)). This increased charge depletion leads to a much smaller ionic radii[16] (Fig. 1(f-bottom)) leading to faster Sn diffusion in HfO_2 compared to Ag and Cu. The predicted low diffusion barrier for Sn in HfO_2, coupled with the relatively low oxide heat of formation and cohesive energy imply that Sn can potentially be a good candidate for filament based non-volatile memories.

Vertical (micron-sized and) nanometer-sized MIM devices in a crossbar geometry were fabricated on SiO_2 (300 nm thick)/Si substrates. The sputter deposited bottom electrodes, Cr/Pt (5 nm/50 nm), were patterned using (photolithography) electron-beam lithography and lift-off process. Plasma enhanced chemical vapor deposition (PECVD) was then used to deposit ~100 nm thick SiO_2 field oxide on the Cr/Pt electrode array, followed by dry etch to open windows down to the Cr/Pt in the field oxide. Atomic layer deposition (ALD) was then used to conformally deposit HfO_2 (4 nm thick, 200 °C, Tetrakis(ethylmethylamino)hafnium (TEMAHf) from PURATREM and H_2O precursor) in the windows, followed by the lithography, sputter deposition and lift-off of the Sn (50 nm) top electrode and a Au capping layer. This resulted in a Cr/Pt/HfO_2/Sn/Au device stack with HfO_2 acting as the switching medium and the SiO_2 field oxide providing accurate device area definition and isolation. A cross-sectional schematic of a typical device geometry is shown in Fig. 2. The device sizes varied from 100 μm diameter circles down to 100 nm diameter circles. The DC sweeps of the devices were measured using Keysight B1500A semiconductor parameter analyzer. Switching characteristics using pulsed measurements were measured using Keysight 33600A Series Trueform Waveform Generator and Keysight DSO204A Infiniium S-Series oscilloscope. We note here that, a silicon oxide film doped with Sn has been studied for bipolar resistive switching,[18] however the use of Sn as anode (and hence active

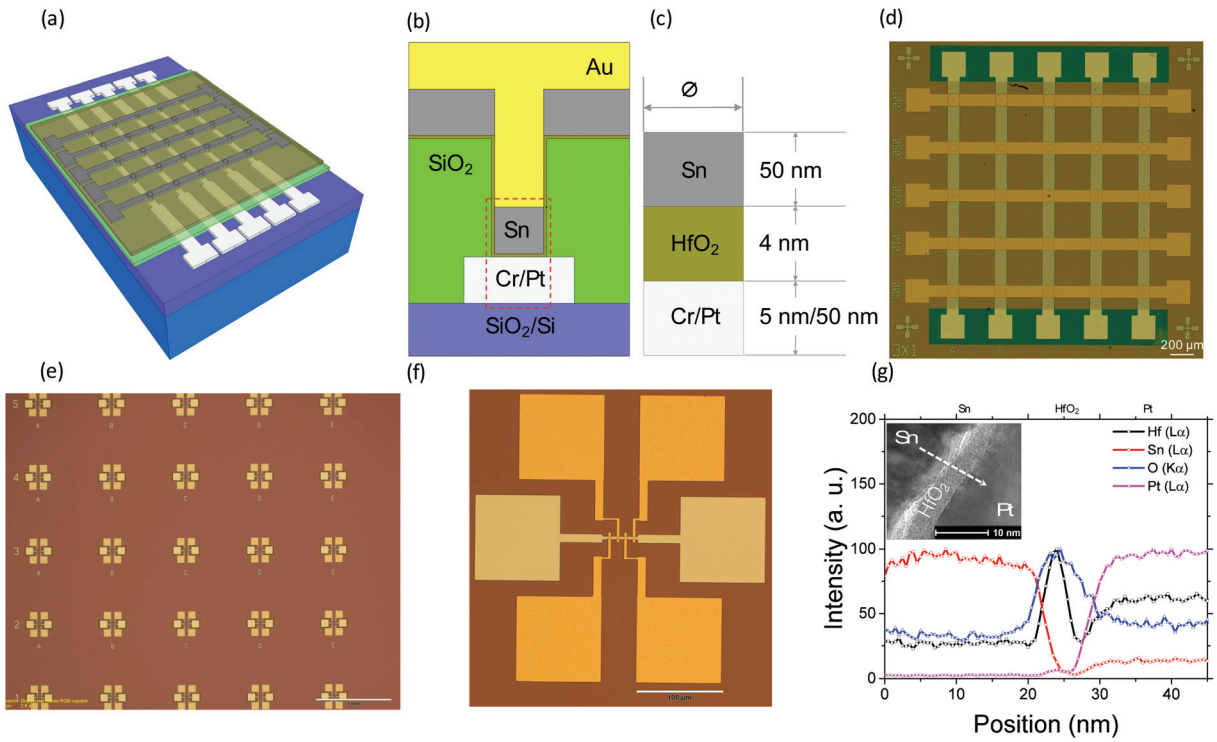

Fig. 2 (a) Schematic showing typical crossbar devices realized on SiO_2/Si substrate. (b) Cross-sectional schematic depicting typical device geometry with Pt bottom electrode, Sn top electrode, Au capping layer and ALD HfO_2 sandwiched in-between. (c) Blown up active device region as marked with red dashed box in (b). Device active region (diameter ϕ) varied from 100 nm to 100 μm. Fully fabricated crossbar structures used in this experiment using photo (d) and e-beam lithography (e, f). Scale bars in (d), (e) and (f) are 200 μm, 1 mm and 100 μm respectively. (e) Cross-sectional Transmission Electron Micrograph (in inset) and corresponding Energy Dispersive X-ray spectroscopy (EDX) line-scan showing Sn|HfO_2|Pt Metal–Insulator–Metal structure. The (energy-dispersive X-ray spectroscopy) EDX mapping was carried on a FEI Talos F200X (S)TEM running at 200 kV equipped with SuperX EDS detector.

filament forming element), borne out of our predictions, has not been demonstrated before even though the use of Sn is benign in Si technology.

Typical response of the as-fabricated devices under electric bias is shown in Fig. 3(a). The as-fabricated devices had a high resistance (typically $>10^{10}$ Ω at 100 mV for all devices). We refer to this as the OFF-state resistance. With positive bias applied to the Sn electrode (forward bias condition, Sn as the anode), the device current increased abruptly to the applied current compliance (100 nA) beyond a threshold voltage (V_{th}). However, the device returned to its high resistance state while sweeping the bias voltage back to zero. On the other hand, no change in the device resistance was observed when positive bias was applied to the Pt electrode (Pt as anode) when the device was operated for the very first time (see Fig. S1†).

However, as shown in Fig. 3(a), when a prior voltage sweep using Sn as the anode was implemented, bidirectional threshold switching was enabled and the device subsequently changed resistance beyond a threshold voltage even when the Pt electrode was used as the anode. This observation is consistent with an electrochemical ionic drift model which would require a small amount of anode metal (Sn) to initially migrate to the vicinity of the Pt electrode for bidirectional switching[19,20] to occur. Such bidirectional volatile switching behavior is useful in selector switch application for large array of cross-point memory. The threshold voltages observed in this study are ~67% higher than devices based on similar thickness of HfO_2 using Cu[21] and Ag[22] anodes. Although, the threshold values measured for our devices are higher than that of Cu and Ag based devices, it is not necessarily a drawback. Rather, in the case of a large array of 1S1R (1 selector-1 resistor) cell, this is advantageous.[23] Too low threshold voltages have a drawback in not providing enough operating window for large array of 1S1R. In fact, in the case where V_{th} is too low ($V_{th} < 1/2V_{cell}$), the selector is unable to prevent sneak current from flowing into unselected cells. $1/2V_{cell}$ is the voltage applied to unselected cells. On the other hand, higher V_{th} can control the sneak current without disturbing the unselected cells. Nevertheless, threshold voltages are subject to the material stack and can be engineered to occur at lower values, if required, for low power applications *e.g.* by means of doping the switching matrix.[24] Large number (100 sweeps) of consecutive DC cycles of the measured threshold switching is shown and the corresponding statistical distribution of V_{th} is shown in Fig. 3(b). The mean ($\bar{x}$) V_{th} found for these devices is 4.13 V (standard deviation, σ = 0.48). It is important for selector switches to withstand the chip operating temperature. In Fig. 3(c) is shown the multiple stable threshold switching measured at 90 °C. The turn-on slope of resistive switching devices is an important parameter. A steep turn-on slope is essential considering their possible use in large, dense cross-bar array as well as novel devices aimed at ultra-scaled operating voltages. The typical turn-on slope observed in Sn-based devices is about 8.75 mV per decade (Fig. 3(c)), being similar

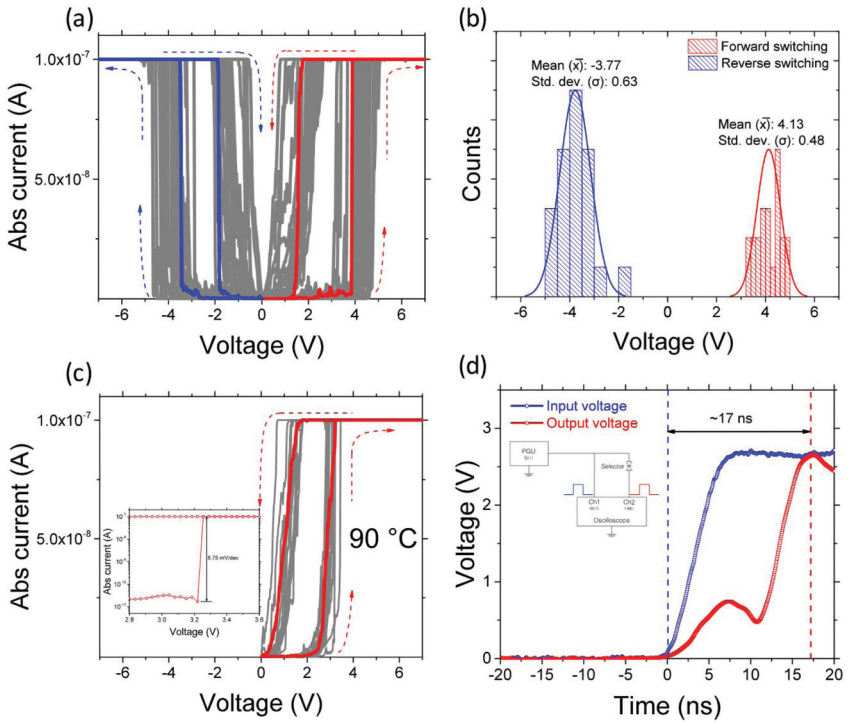

Fig. 3 (a) Unipolar, bidirectional threshold switching. Multiple traces measured in both, forward and reverse direction, are shown. Representative traces are highlighted in red and blue. (b) Statistical distribution of the measured threshold voltages for the traces shown in (a). (c) Cumulative multiple traces measured for stable threshold switching at 90 °C. The red curve shows a representative trace. In inset is shown the representative trace showing steep turn-on slope (8.75 mV dec^{-1}). (d) Pulsed response showing very fast (17 ns) turn-on. In inset is shown the pulsed set-up.

to turn-on slopes for Cu and Ag based devices,[21,22] and is adequate for non-volatile memory applications. There is experimental evidence in CBRAM devices that the pulsewidth required to trigger a set or reset event depends exponentially on the amplitude of the applied pulse.[25–27] Considering this, we used a 4 V amplitude and 50 ns width, with an external pulse generator, and found the switching speed to be about 17 ns (Fig. 3(d)). Cu and Ag based selector devices have shown switching speeds in the same order of magnitude.[21,22] Thus Sn-based resistive switching devices offers similar advantages as Cu and Ag.

In response to the modulation of compliance current (I_{cc}) Sn-based devices exhibit coexistence of threshold and memory switching behavior. This is due to the inverse relationship between the read resistance (post the device turn ON) in resistive switching device and the set compliance current commonly observed. Similar behavior has been reported in other resistive switching devices (ref. 28 and references therein). This can be more simply understood in the case of cationic filamentary devices by considering that a larger compliance current would supply more metal ions to form a stronger conducting filament when the low resistance state occurs. This explanation is experimentally supported through observation of an increase in physical volume of the conducting filament with increased compliance current.[29]

Fig. 4(a) shows the bipolar memory switching behavior. A large number (150 sweeps) of measured consecutive DC cycles is shown in Fig. 4(a) along with the statistical distribution for V_{Set} and V_{Reset}. The mean ($\bar{x}$) V_{Set} and V_{Reset} found for these devices is 3.36 V (standard deviation, σ = 0.42) and 1.46 V (standard deviation, σ = 0.31). Also, the mean ($\bar{x}$) current measured at high resistance state (I_{HRS}) is 4.58×10^{-12} A (standard deviation, σ = 1.46×10^{-11} A). A data retention time longer than ten years is expected for nonvolatile memory. Extensive time dependent measurement of stable retention data collected for Sn-based nonvolatile memory are presented in Fig. 4(c). The resistance of the high and low resistive states was determined by measuring the current at a small bias of

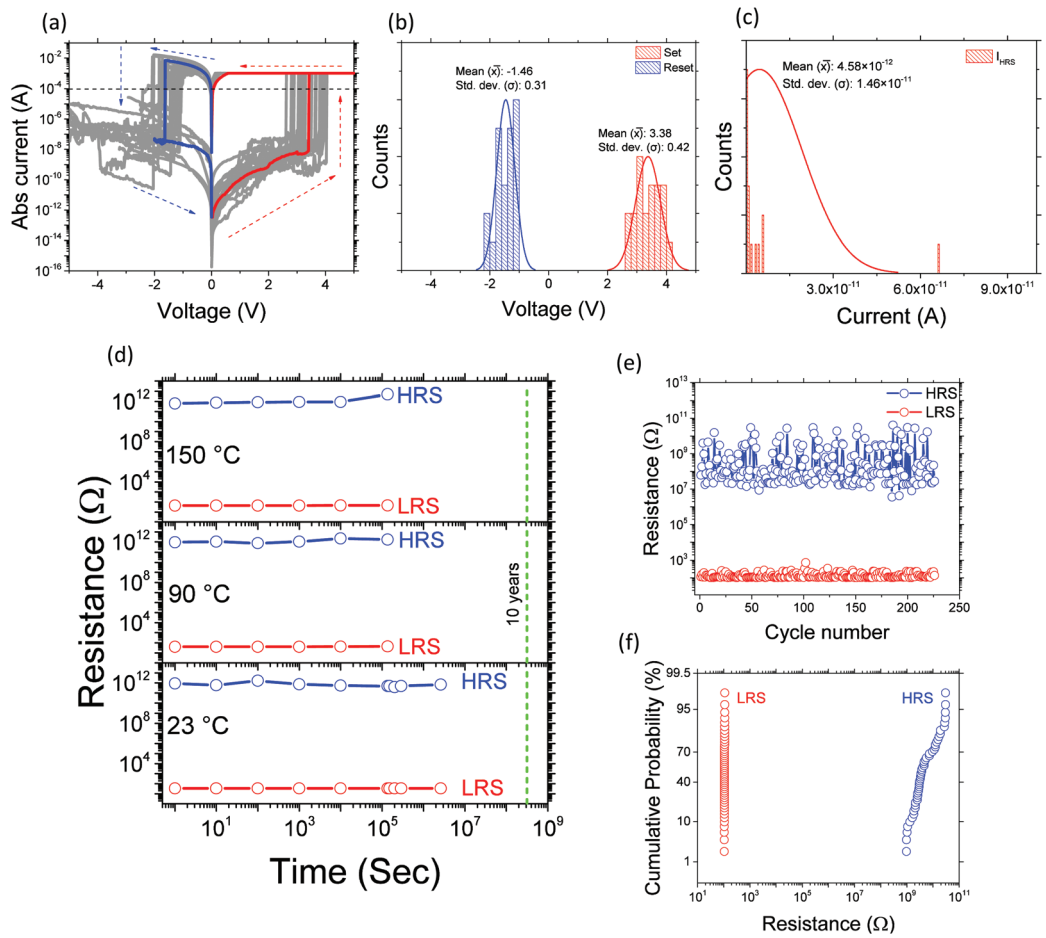

Fig. 4 (a) Memory switching achieved by increasing the compliance current to 1 mA. Multiple cumulative traces measured for both, Set and Reset conditions, are shown. Representative traces are highlighted in red and blue. (b) Statistical distribution of the measured threshold voltages for the traces shown in (a). (c) Statistical distribution for current measured at high resistance state (I_{HRS}) in (a). (d) Extensive memory retention study. Time dependent stable retention measured at 23 °C, 90 °C and 150 °C. (e) Cycling endurance over 225 manual DC switching cycles. (f) Distribution of LRS and HRS.

100 mV. The ratio of the high resistive to low resistive state (the "memory window"), as can be seen from Fig. 4(c) is $>10^{10}$. This is similar to, or larger than the ON/OFF ratios (10^7) for cationic filamentary devices reported in Cu/HfO_2 [21] and Ag/HfO_2 [22] systems. Considering that the memory retention must withstand thermal stresses, measurements were performed at room temperature as well as elevated temperatures, 90 °C (chip operating temperature) and 150 °C. Very stable retention ($\bar{x}_{HRS} = 7 \times 10^{11}$ Ω, $\sigma_{HRS} = 3.69 \times 10^{11}$, $\bar{x}_{LRS} = 34.57$ Ω, $\sigma_{LRS} = 0.18$ at 23 °C, $\bar{x}_{HRS} = 1.28 \times 10^{12}$ Ω, $\sigma_{HRS} = 5.64 \times 10^{11}$, $\bar{x}_{LRS} = 40.90$ Ω, $\sigma_{LRS} = 1.24$ at 90 °C, $\bar{x}_{HRS} = 1.48 \times 10^{12}$ Ω, $\sigma_{HRS} = 1.68 \times 10^{12}$, $\bar{x}_{LRS} = 44.97$ Ω, $\sigma_{LRS} = 0.76$ at 150 °C) that withstood thermal as well as small electrical stresses of read voltages (100 mV) was observed. Sn_2O being more stable under thermal stresses (considering Sn_2O has more negative heat of oxide formation compared to Cu_2O, Ag_2O) than Cu_2O and Ag_2O (refer to Fig. 1(c)) Sn-based devices are potentially advantageous in achieving stable resistive switching performance over a longer period of time than Cu or Ag electrodes. This is deduced from the fact that interfacial oxide between the anode and switching matrix plays an important role in filament formation, as explained earlier. Retention of non-volatile states, lasting up to four weeks (for room temperature and 40 hours each for elevated temperatures) as tested, is already sufficient for certain neuromorphic applications involving short and medium term plasticity.[30] Among the highest priority for CBRAM devices is the cycling endurance since this is amongst the strongest concerns for the device reliability.[17] The manual endurance data (225 DC cycles) presented in Fig. 4(e) may not yet meet the standards set forth by other resistive switching devices.[17] However, Sn-based CBRAM devices are in the initial phases of development and achieving endurance $>10^6$ cycles by pulsed cycling endurance test will be of importance for practical applications and hence will be focus of future studies. In this study we have successfully demonstrated use of Sn as the filament forming species in oxide matrix. However, Sn anode can also be potentially used in chalcogenide based resistive switching devices. The Sn anode can either be used to instigate a phase change, Phase change memory (PCM), in GeTe or Ge_2Se_3 films or simply as migrating ion source for CBRAM memory.[31] The switching mechanism is discussed next.

Fig. 5(a) illustrates a typical time dependent response of the measured current through the devices under constant voltage stress. The voltage stress is varied (Fig. 5(b)) from 0.5 V to 2.5 V, the threshold at which the resistive state changes abruptly. The temporal response of the current follows three stages (Fig. 5(c)): (i) an initial decrease that varies as t^n (with $n \sim -0.72$ to -0.08 as the voltage increases from 0.5 V to 2.25 V, see Fig. S2 in ESI†), (ii) a gradual increase in current, followed by (iii) a sharp increase indicative of an abrupt change in the resistive state. For low voltages, stages (ii) and (iii) do not appear. This incubation time leading to stage (iii) is inversely proportional to the voltage. The initial decrease (stage (i)) has been associated with dielectric relaxation pro-

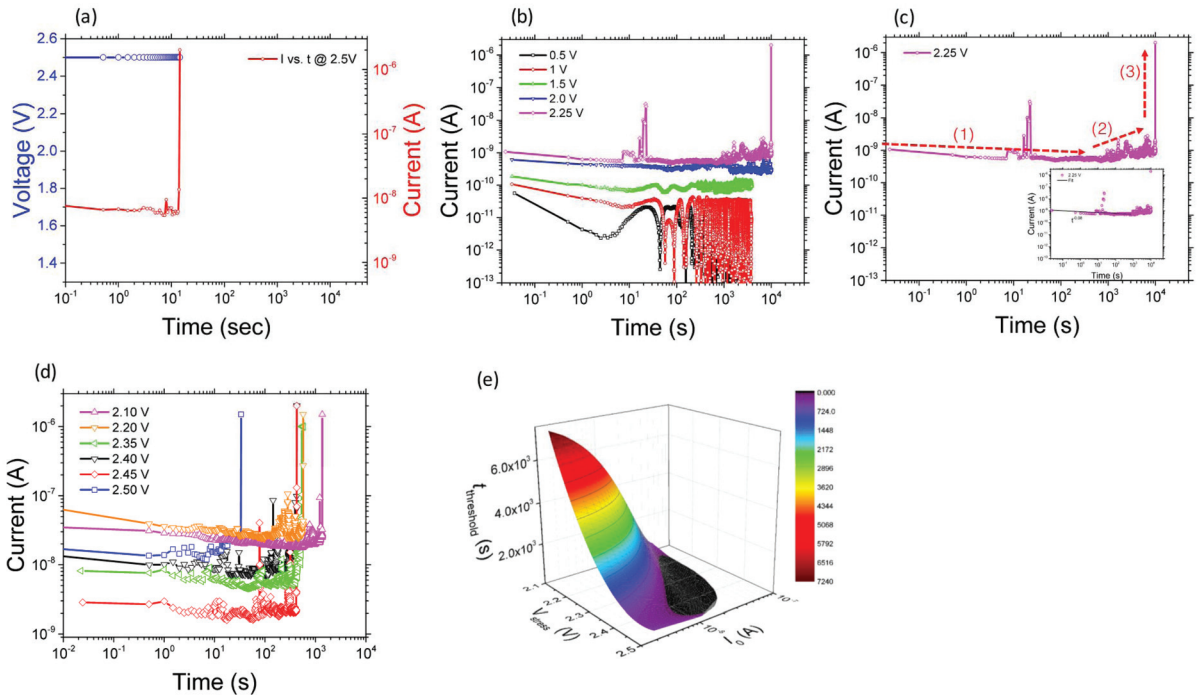

Fig. 5 (a) Typical time domain response of the devices under constant voltage stress. (b) Time domain response under gradual voltage stress. The filament does not form until a certain threshold voltage stress is reached, 2.25 V in this case. (c) Three regimes of filament formation. In inset is shown the fit for regime 1, a power law decay $t^{-0.08}$, indicating a dielectric relaxation process that involves dipole as well as charge carrier relaxation. (d) Time domain device response under voltage stress above the $V_{stress\text{-}min}$. (e) 3D plot showing dependence of time to threshold on the voltage stress and the starting leakage current at $t = 0$ (I_0).

cesses and the creation of charge traps.[32] The slight increase in current in stage (ii) is not clearly understood but may be related to stress-induced-leakage-current (SILC).[33] Stage (iii) is indicative of the formation of the conducting bridge.

It is clear from the data in Fig. 5(d) that as V increases, the time to reach stage (iii) *i.e.* the formation of the conducting filament, reduces. One notes that the different traces in Fig. 5(d) are for a number of different devices with differing amounts of starting current values (I_0). The differences in the starting currents are ascribed to small differences in the starting microstructure of the materials. A few key conclusions may be made from this data. Firstly, the observation of a time to threshold that is voltage dependent is consistent with a filament formation mechanism that is diffusive and activation energy barrier limited. The probability of a defect surmounting an energy barrier is given by

$$P \propto \nu e \frac{E_B - qV}{kT} \quad (1)$$

where ν is the frequency at which the charged defect (with charge q) attempts at "jumping" across the barrier, E_B is the height of the energy barrier that is reduced by the application of an electrical potential V seen by the defect. Therefore, the higher the applied voltage across the film, the higher the rates at which the defect hops from site to site. Additionally, it is also seen that a certain minimum voltage (V_{min}) is required to induce filament formation. As can be seen in Fig. 5(d), the minimum voltage stress required is ~2.1 V in our case.

The second important observation addresses the issue of variability that is observed in all of the filamentary breakdown devices seen to date, and links the variability to differences in the starting local microstructure of the device. The plot in Fig. 5(e) represents the time required for filament formation as a function of two variables: the applied voltage (V_{stress}) and the starting current (I_0) at time, t = 0. As can be seen the time to threshold is dependent on not only the V_{stress}, but also on the I_0. Lower I_0 and smaller V_{stress} results in longer time to threshold. It clearly indicates that local microstructures from device to device are different – hence the different starting currents – and that then clearly affects the filament formation. The observations are consistent with a model where the filament initiates at heterogeneous centers in the device that are created by variations in the oxide microstructure, and that their growth and configuration is different from device to device, leading to the observed variability.

In summary, we present a criterion for electrode metal selection applicable to cationic filamentary devices. In general, the criterion indicates that small cohesive energy (E_c), low heat of formation of metal oxide (ΔH) and small ionic radius are preferable for low energy cationic filament formation. Based on this criterion we then successfully identify and demonstrate the viability of Sn|HfO_2 based CBRAM devices. Comparable device performance to Cu|HfO_2 and Ag|HfO_2 devices which include a turn-on voltage of ~3.4 V, a steep turn-on slope (8.75 mV per decade) and very fast switching (17 ns), establishes Sn|HfO_2 based CBRAM devices a good alternative to Cu and Ag anodes. We argue that Sn, being isovalent with Si, has the distinct advantage of being compatible with Si CMOS technology, unlike Cu and Ag which are fast diffusers, contribute to electronic defect states, and require diffusion barriers and liners for incorporating into the back end of Si CMOS, and are likely incompatible for front-end applications. Use of Sn is well justified also by first principle calculations that elucidates the preferred atomistic pathways and lower diffusion barriers compared to Cu and Ag. Threshold and memory switching can be achieved by modulating the compliance current through the device. Time domain response to subthreshold voltage stress gives insights into the filament formation process, revealing the dependency of time to threshold on the applied voltage as well as the initial leakage current through the device.

Nudged elastic band calculations, charge density difference and Bader charges from density functional theory

Density functional theory (DFT) calculations were carried out using the Vienna *Ab initio* Simulation Package (VASP).[34–36] The projector augmented wave method was applied to describe the interactions between valence electrons and frozen cores.[37] An energy cutoff of 600 eV was used. All calculations used spin-polarized DFT. The Perdew–Burke–Ernzerhof (PBE)[38] form of the generalized gradient approximation (GGA) was used to describe the exchange and correlation interactions. The Gaussian smearing method with a width of 0.1 eV around the Fermi level was applied to facilitate convergence. The electronic energies were converged to 10^{-6} eV. Ionic relaxations were performed until the residual forces on ions were less than 0.02 eV $Å^{-1}$. A 1 × 1 × 1 Γ-centered k-point mesh was chosen to reduce the computational cost. The nudged elastic band (NEB)[39–42] method with climbing images was used for diffusion energy barrier calculations. We have computed the charge density difference for the transition state along the diffusion pathway. We divided the system into two subsystems for the charge density difference (CDD) calculations, using the Cu/Ag/Sn as one subsystem and the HfO_2 as the second subsystem. Bader charges were also computed for the various ions in HfO_2.

Author contribution

S. S. conceived the project, designed the criterion for electrode metal selection and experiment, fabricated devices and performed electrical characterization. B. C., J. L., L. S., R. D., L. E. O., D. R., participated in various aspects of crossbar device fabrication. Y. L. performed the cross-sectional TEM analysis. K. S., P. C. and S. K. R. S. S. performed the DFT calculations. K.N. and S.D. helped setup the electrical cycling endurance measurement. S. S. and S. G. co-wrote the manuscript. All authors commented on the manuscript.

Conflicts of interest

There are no conflicts to declare.

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